

FEB-19-2004 (THU) 13:29 GALLAGHER & LATHROP

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FEB 20 2004

Applicants: Masahiro Ishida, et al.  
Serial No.: 09/699,077  
Filing Date: October 27, 2000  
Title: Method and Apparatus for  
Fault Simulation of  
Semiconductor Integrated  
Circuit

Examiner: Ayal Sharon  
Art Unit: 2123

OFFICIAL  
STL/A  
2/26/04  
g-26/04/04

February 19, 2004  
San Francisco, California

Mail Stop Non-Fee Amendment  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This communication is submitted in response to the office action mailed November 20, 2003  
(referred to herein as "Office Action").

Docket: KPO089

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PAGE 1/9 \* RCVD AT 2/19/2004 4:28:55 PM [Eastern Standard Time] \* SVR:USPTO-EFXRF-1/4 \* DNIS:8729306 \* CSID:415 989 0910 \* DURATION (mm:ss):02:44